of the electrodes, heavily doped regions with the same conductivity type beneath the electrodes can be used and these heavily doped regions are defaulted in all the figures. In addition, in FIGS. **3**, **4** and **6**, the anode contacts A (or cathode K) can be either made at the bottom of the substrate, or made at the top of a p (or n)-region **9**.

2) High-voltage bipolar transistors. This can be done by using a p^{+} (^{or} n^{+})-region serving as emitter E, which is inserted in the middle of region **2** in FIGS. **3–7**. Region **2** itself is the base B, and the collector C is made on region **9**. FIG. **10** shows an example of high-side-control vertical transistors using the surface voltage sustaining structure of FIG. **3**. In this example, a region **14** as emitter E is formed in the middle potion of region **2**.

3) High voltage lateral junction field effect transistor (JFET). This can be done by using the middle of region **2** in FIGS. **3–7** as the drain D. FIG. **11** shows an example of a JFET using the surface voltage sustaining structure of FIG. **3**. The source S is formed at the end of the surface voltage sustaining structure. The source contact is not only connected directly to region **2** at the ends of the surface voltage sustaining structure, but also connected through region **9** to the substrate. The gate is made on the p-region at the ends of the surface voltage sustaining structure (region **8**) through a p^{+}-region **11**, which serves for the contact of the gate G. The conduction of the channel (**2**) beneath region **8** is controlled by the gate voltage applied to region **8**.

4) High voltage lateral metal-oxide-semiconductor field effect transistor (MOSFET). FIG. **12** shows an example of a MOSFET using the surface voltage sustaining structure of FIG. **7**. The drain D of the MOST can be made the same as in JFET. A n^{+}-region **13** serving as the source S is set in region **9** which serves as the source-body. The source electrode contacts both region **13** and region **9**. The gate G is set on the top of an oxide layer **12** which is formed on the semiconductor surface. The gate is extended from region **13** to a part of region **2** beyond the surface voltage sustaining structure, which has no region with opposite conductivity type on its top. The ionized impurities of this part has no appreciable effect to the field profile around the peak, because this part is very short and the electric flux produced by them are mostly terminated immediately by their induced charges at region **9** and the p^{+}-buried region **10**.

The MOSFET using the structure of FIG. **7** yields a very low on-resistance besides high breakdown voltage.

The inventor has investigated a 0.8 μm BiCMOS technology and found that a breakdown voltage of 90% of that of the parallel plane junction with the same substrate doping concentration can be reached by using the surface voltage-sustaining structure shown in FIG. **3**, and the lateral MOSFET with this surface voltage sustaining structure has low on-resistance, high respond speed and large current density. The figure of merit FM of this kind of lateral MOSFET is:

$$FM \equiv \frac{(\text{breakdown voltage}) \times (\text{current density})}{(\text{turn-off time})} \approx 18\ \text{kV} \cdot \text{A/cm}^2 \cdot \mu\text{S}$$

which is 250 times of that of the conventional lateral MOSFET.

5) High voltage insulated gate bipolar transistor (IGBT). This can be made like MOSFET. The differences to the MOSFET are as follows: A p^{+}-region **14** serving as anode A (o rcathode K) is set at the middle top of region **2**; the cathode K (or anode A) is set as the same as the source in the said lateral MOST.

FIG. **13** shows the cross-section of an IGBT using the surface voltage sustaining structure of FIG. **3**.

An example of processing the structure shown in FIG. **13** is following: 1) starting with a p^{-}-substrate **1** of doping concentration around 1×10^{15} cm^{-3} and ion-implanting Boron with dose around 4×10^{12} cm^{-2} for buried layer **10**; 2) epitaxying an n^{-}-layer with thickness around 1 μm over the sustrate 1; 3) ion- implanting phosphor with dose around 3×10^{12} cm^{2} for region **2**, which has a Gaussian distribution with peak around 0.8 μm in depth and spread around 0.4 μm after the whole processing; 4) ion-implanting Boron with dose around 2×10^{12} cm^{-2} for region **8** and region **9**, wherein region **8** has the Gaussian distribution with peak at the surface and spread around 0.4 μm; 5) ion-implanting boron with dose around 1×10^{12} cm^{-2} for region **6** and region **9**; 6) ion-implanting Boron with dose around 1.7×10^{12} cm^{-2} for region **7**. The remaining processes are abbreviated since these processes are normal processes known by those skilled in the art. Regions **6** and **7** have the same depth and spread as region **8**. All of the ion-implantation stated above are effected through adequate masks. Region **9** is a pure p-region because of said steps of 1), 4), and 5).

In this invention, the compensation effect of the regions with opposite conductivity type is used in the surface voltage sustaining structure to approach the ideal field profile. This method has three advantages: (1) high breakdown voltage; (2) the flexibility in technology and the compatibility with the sub-micron technology; (3) the low on-resistance of the lateral MOSFET's or the low base resistance of the vertical bipolar transistor due to that the regions of opposite conductivity type in the structure are not fully depleted in the on-state. Obviously, high voltage integrated circuits (HVIC's) and power integrated circuits (PIC's) can be implemented with low costs and high performances by using this invention.

Evidently, the surface voltage sustaining structure of this invention can also apply to the case of a semiconductor on insulator on semiconductor (SIS) as far as the substrate is electrically connected to a structure outside of the surface voltage-sustaining structure.

In addition, the requirement of that the effective donor (or acceptor) density decreases with the distance to the center of structure **2** can also be implemented by using many small zones of a constant doping density of n (or p)-type.

Although the invention has been described and illustrated with reference to specific embodiments thereof, it is not intended that the invention be limited to these illustrative embodiments. Those skilled in the art will recognize that modifications and variations can be made without departing from the spirit of the invention. For example, the conductivity of the substrate and doped regions may be opposite of those illustrated herein. Therefore, it is intended that this invention encompass all such variations and modifications as fall within the scope of the appended claims.

I claim:

1. A surface voltage sustaining structure for a semiconductor device comprising a first semiconductor region of a second conductivity type formed on a second semiconductor region of a first conductivity type, said first semiconductor region being doped at a higher density of impurities than said second semiconductor region, said surface voltage sustaining structure comprising a third semiconductor region formed around said first semiconductor region, said third semiconductor region having an average doping density of the second conductivity type that decreases from a